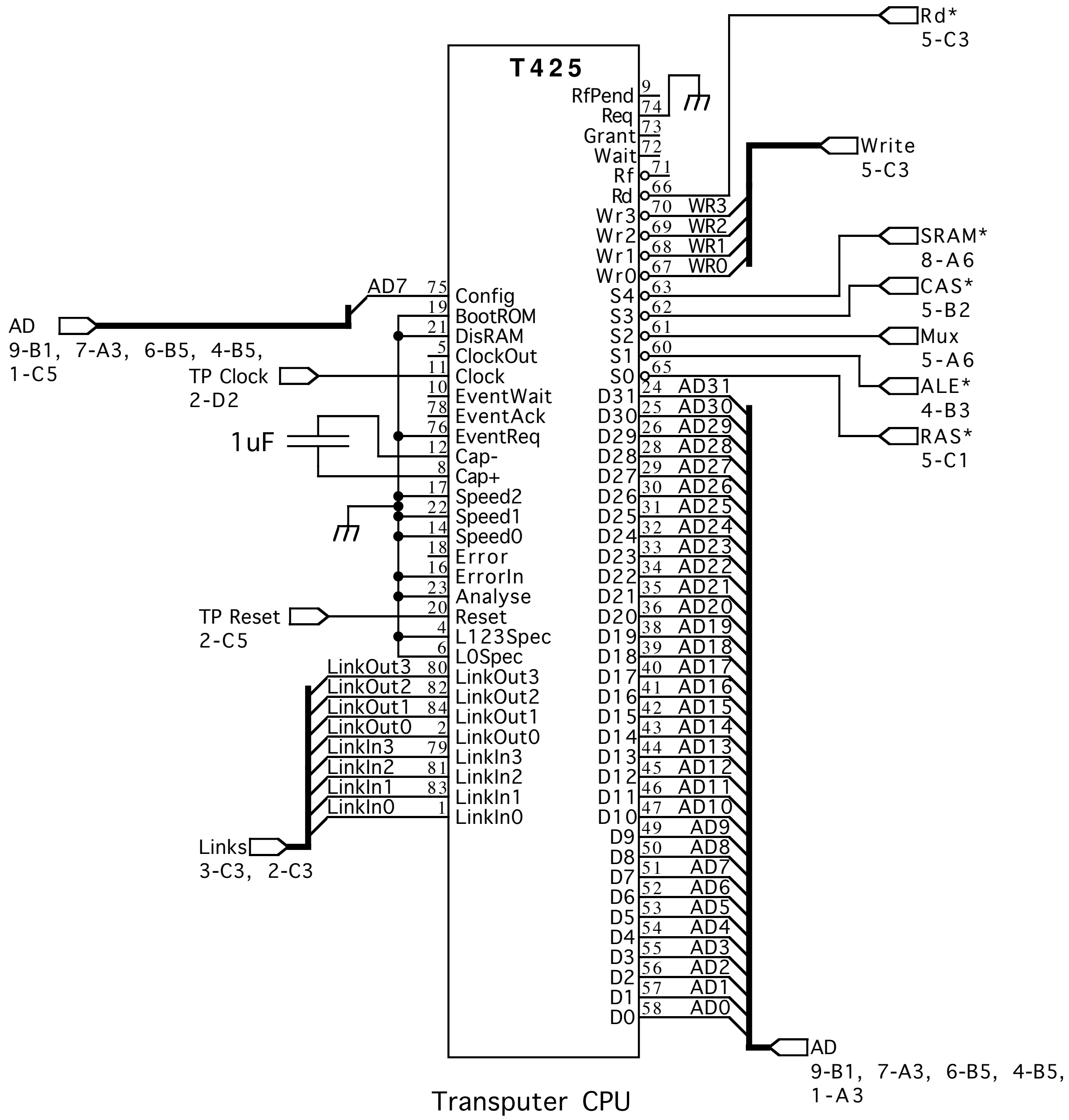
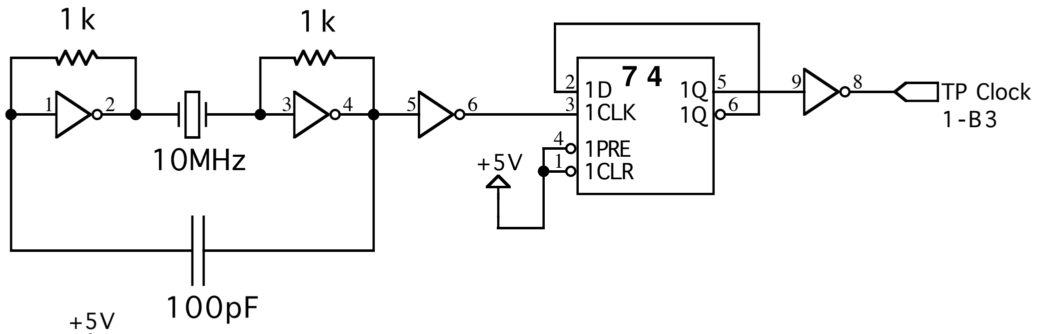
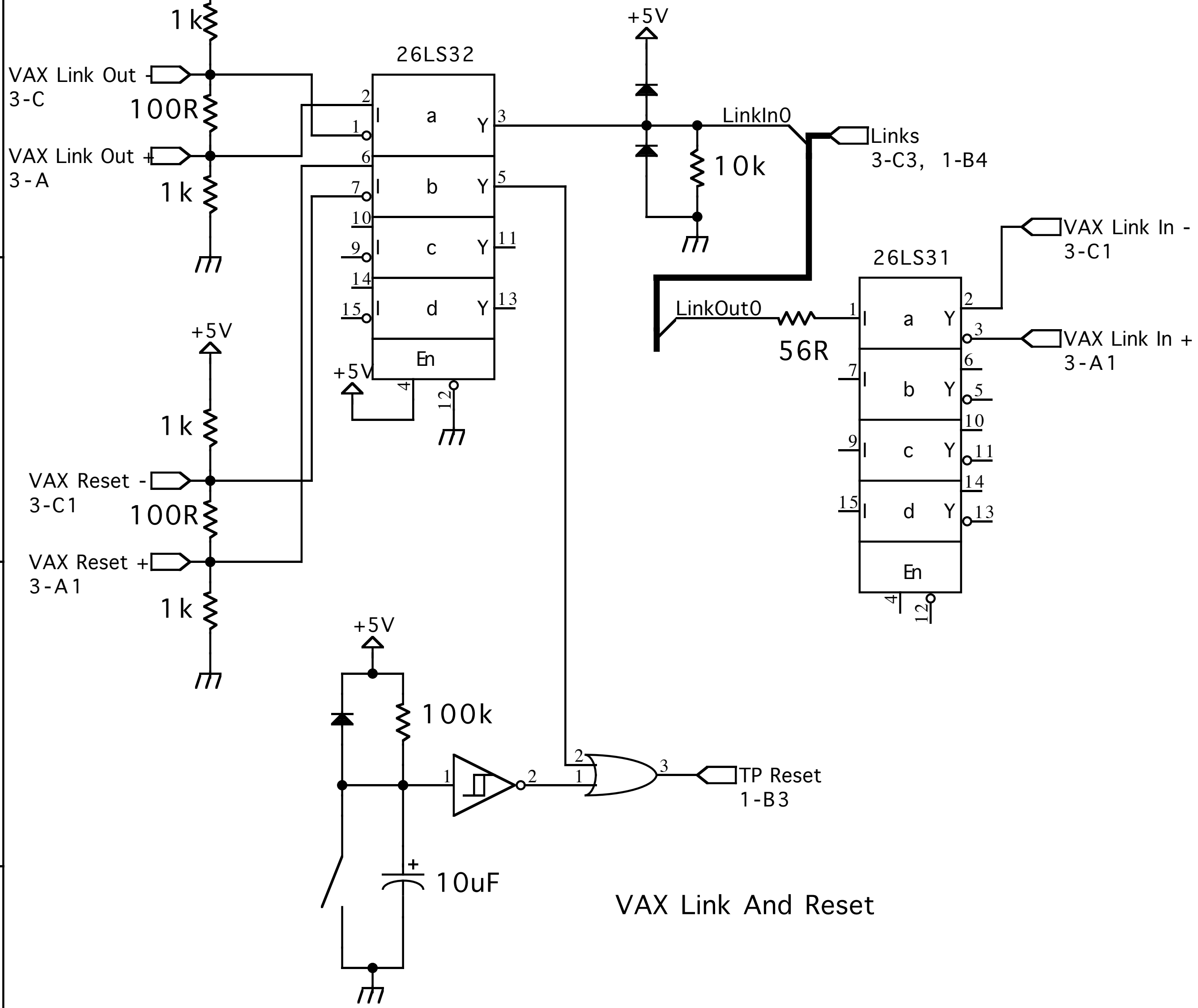


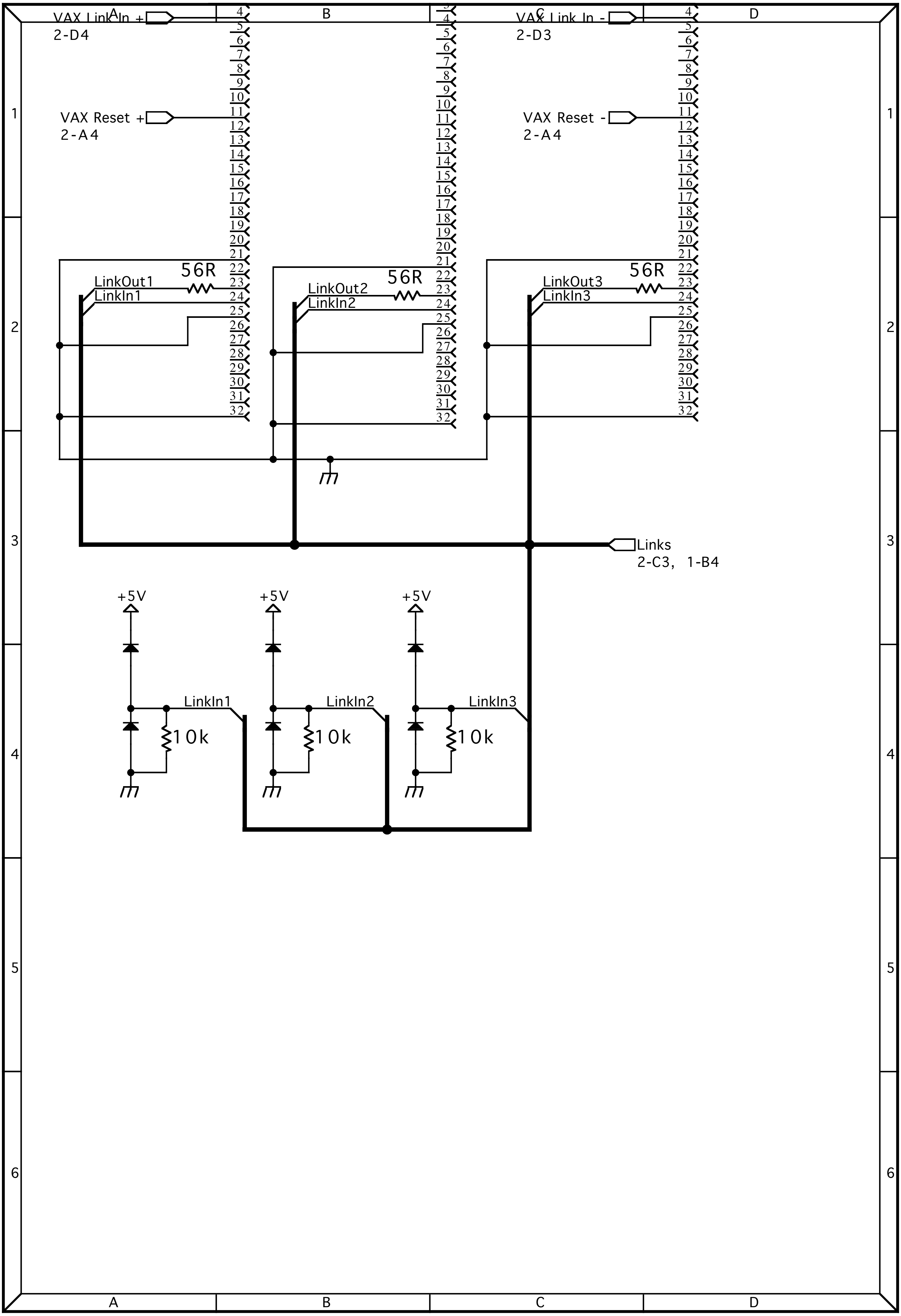
Transputer CPU



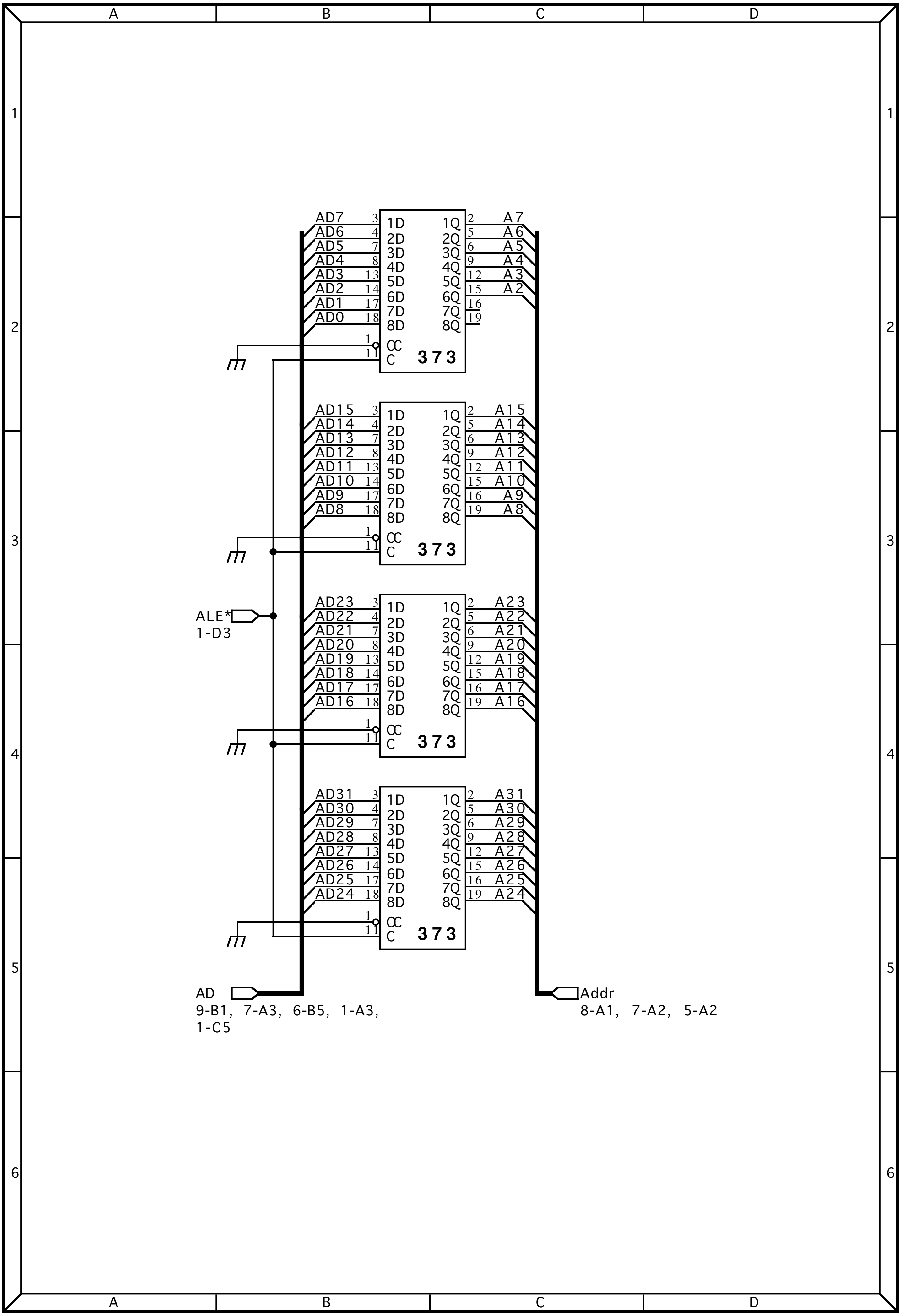
5MHz Transputer Clock



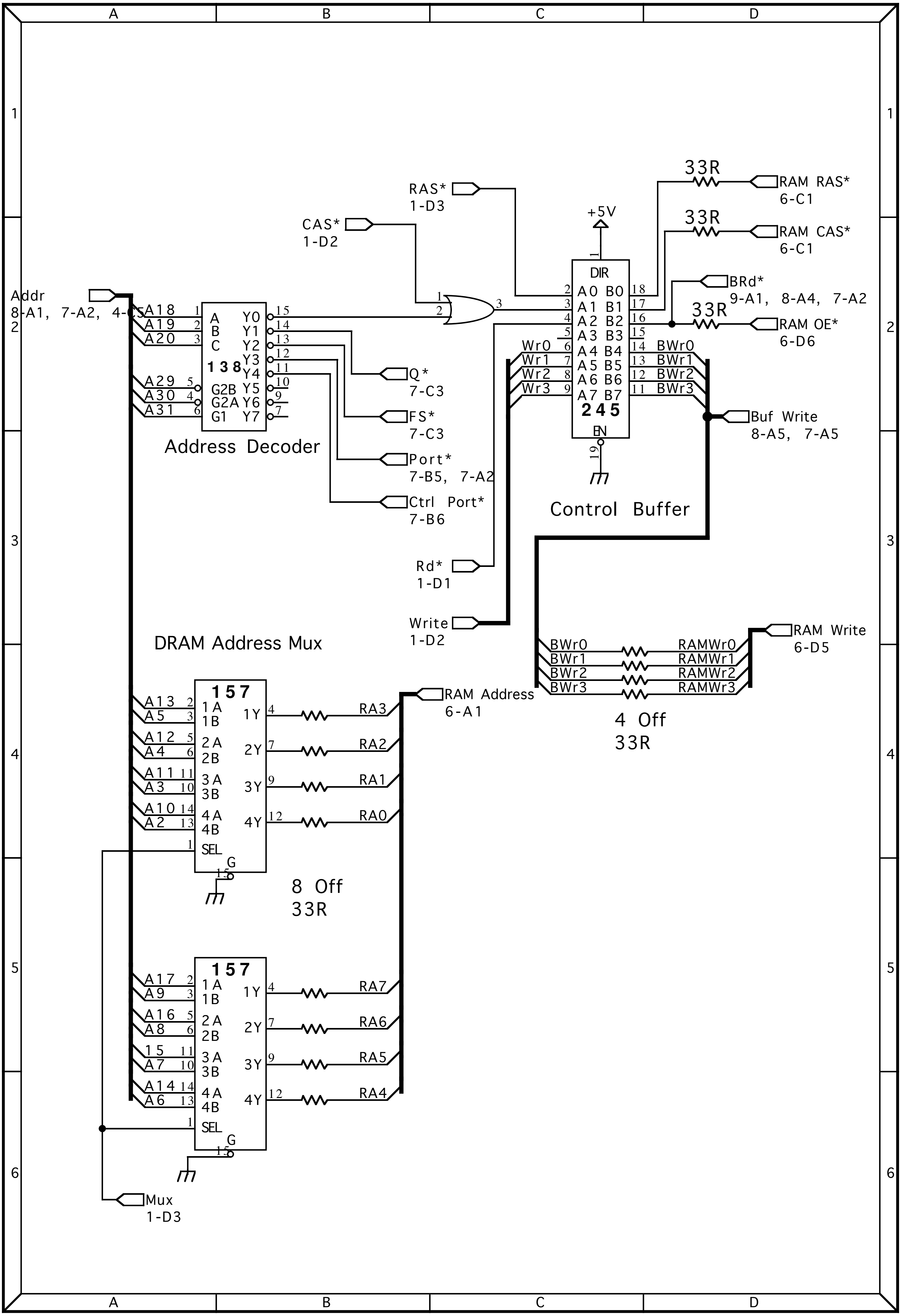
VAX Link And Reset

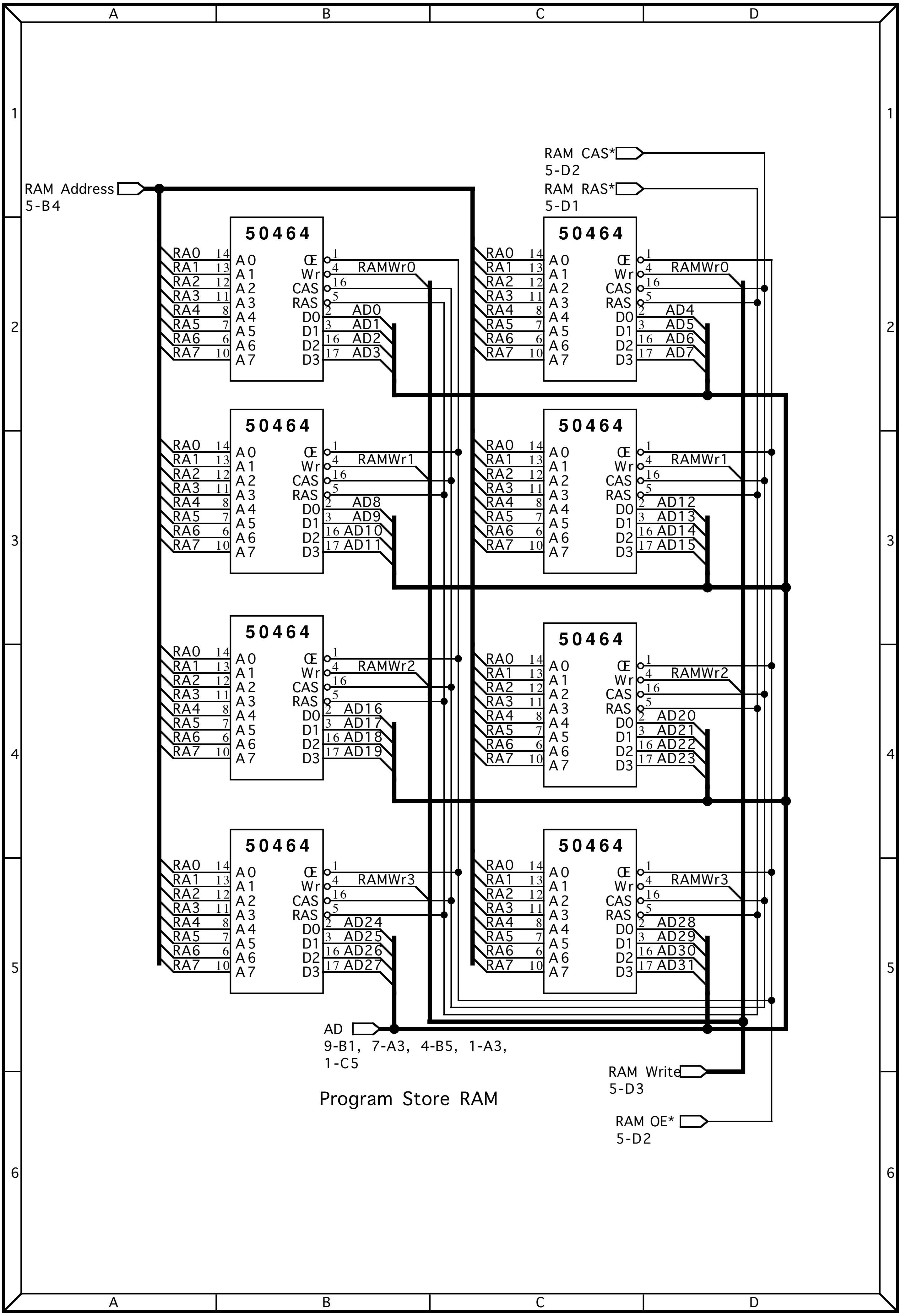


VAX Link In +
2-D4
VAX Reset +
2-A4
VAX Link In -
2-D3
VAX Reset -
2-A4
LinkOut1
LinkIn1
56R
LinkOut2
LinkIn2
56R
LinkOut3
LinkIn3
56R
Links
2-C3, 1-B4
+5V
+5V
+5V
LinkIn1
10k
LinkIn2
10k
LinkIn3
10k

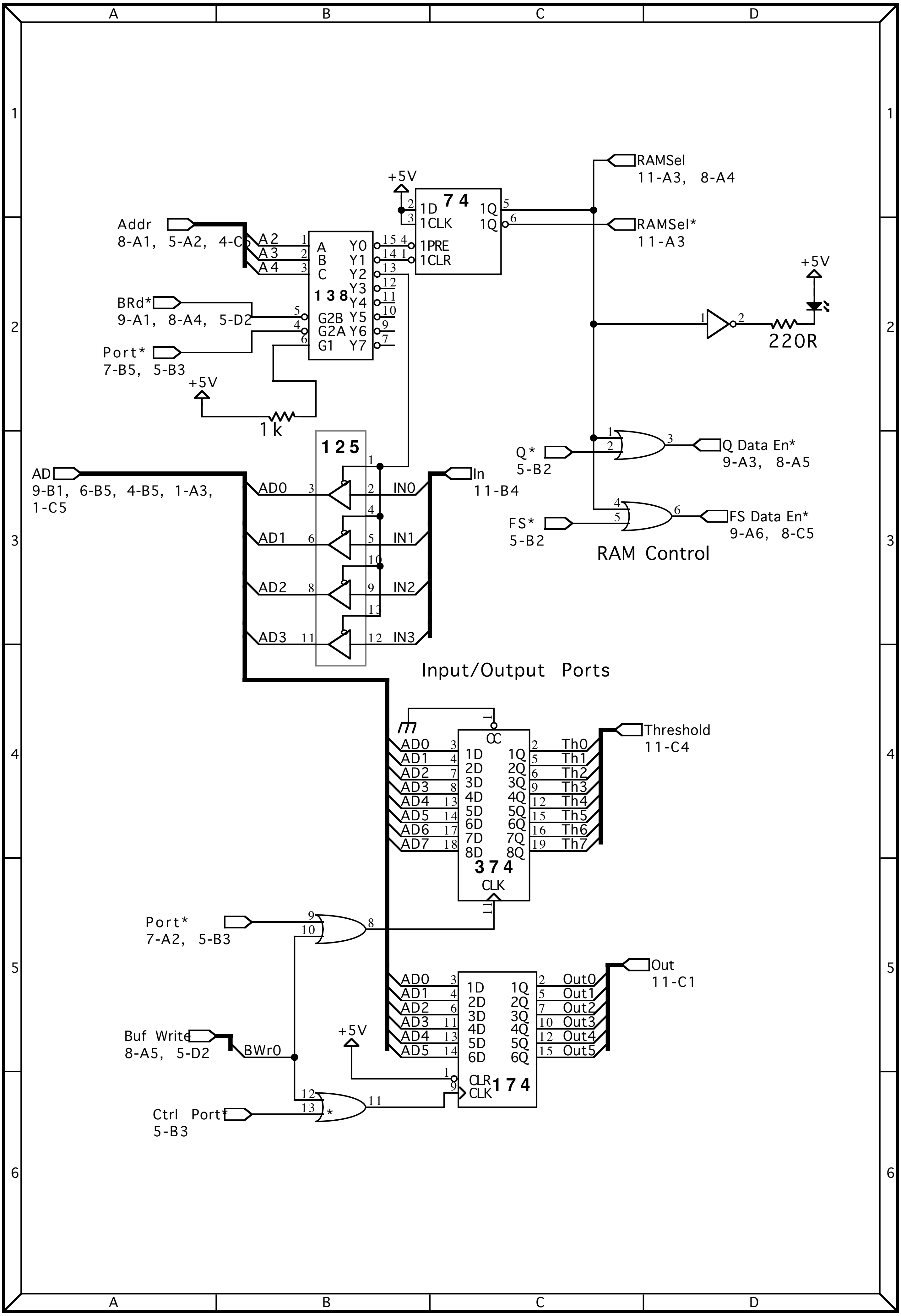


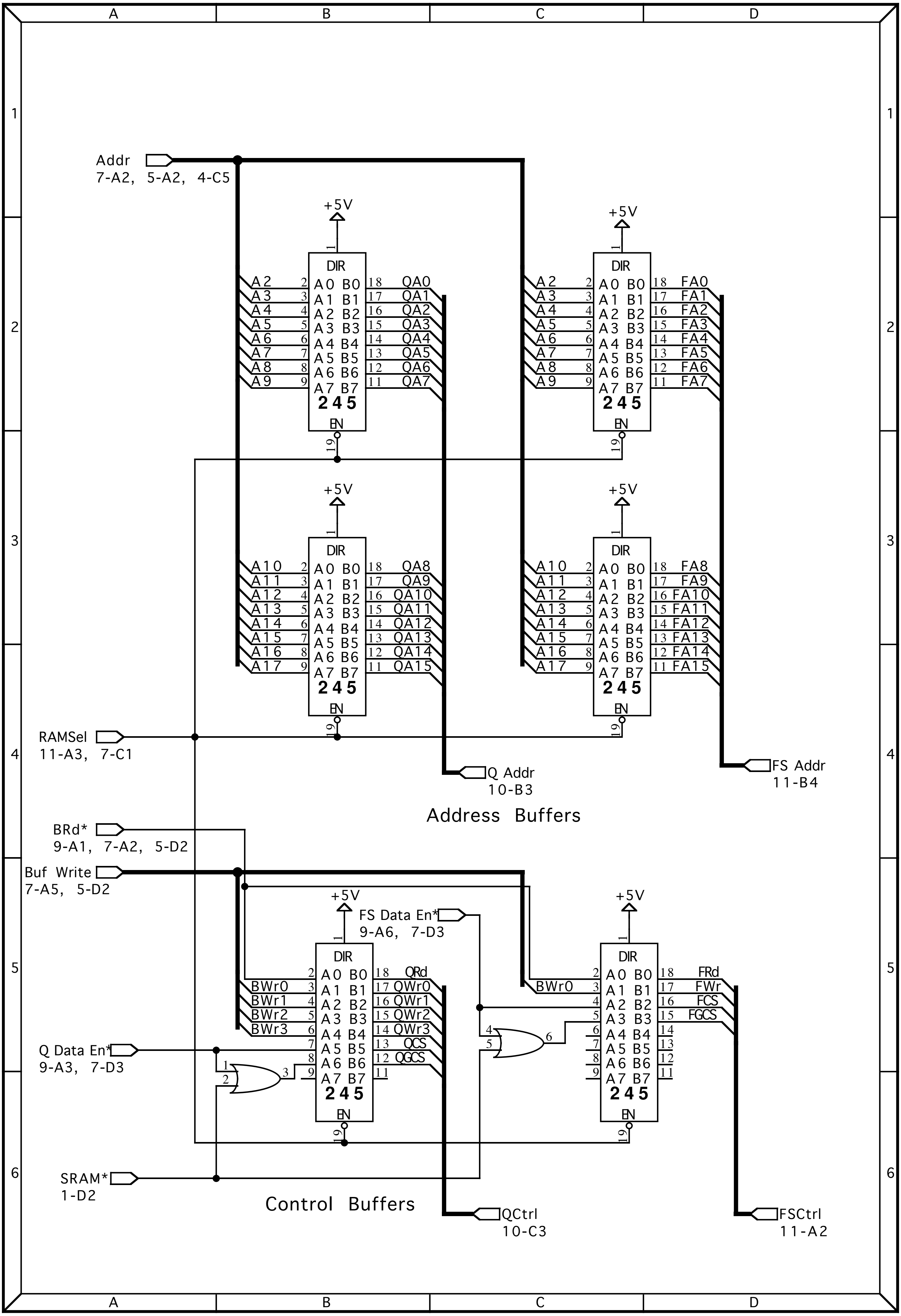
A
B
C
D
1
2
3
4
5
6
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
1D
2D
3D
4D
5D
6D
7D
8D
OC
C
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
373
A7
A6
A5
A4
A3
A2
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
A15
A14
A13
A12
A11
A10
A9
A8
ALE*
1-D3
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
A23
A22
A21
A20
A19
A18
A17
A16
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
A31
A30
A29
A28
A27
A26
A25
A24
AD
9-B1, 7-A3, 6-B5, 1-A3, 1-C5
Addr
8-A1, 7-A2, 5-A2

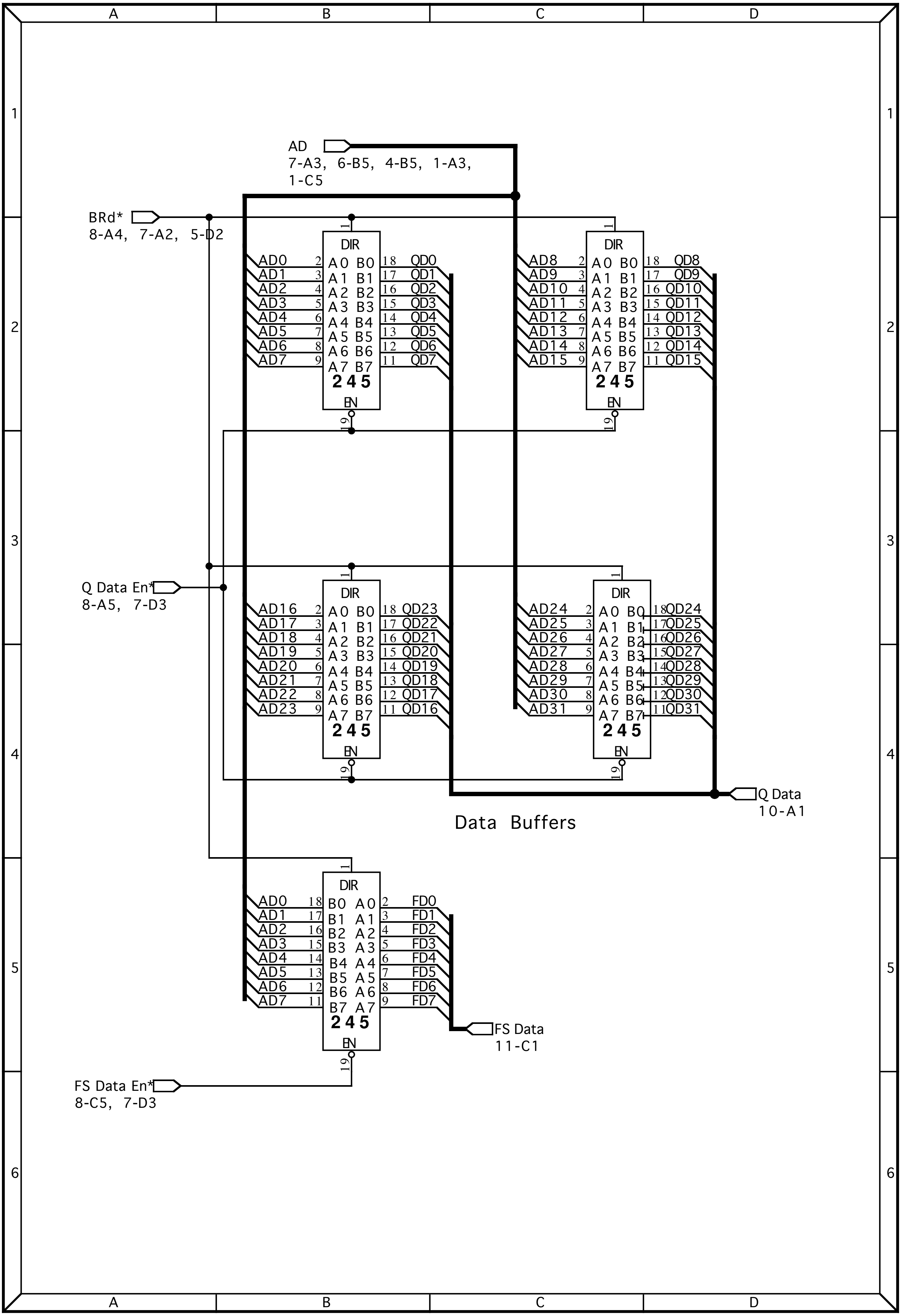

A
B
C
D
1
2
3
4
5
6
Addr
8-A1, 7-A2, 4-C5
A18
A19
A20
A29
A30
A31
138
Address Decoder
RAS*
1-D3
CAS*
1-D2
+5V
DIR
245
EN
33R
RAM RAS*
6-C1
RAM CAS*
6-C1
BRd*
9-A1, 8-A4, 7-A2
RAM OE*
6-D6
Wr0
Wr1
Wr2
Wr3
BWr0
BWr1
BWr2
BWr3
Buf Write
8-A5, 7-A5
Q*
7-C3
FS*
7-C3
Port*
7-B5, 7-A2
Ctrl Port*
7-B6
Control Buffer
Rd*
1-D1
Write
1-D2
DRAM Address Mux
RAMWr0
RAMWr1
RAMWr2
RAMWr3
RAM Write
6-D5
4 Off
33R
157
RAM Address
6-A1
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
8 Off
33R
SEL
Mux
1-D3



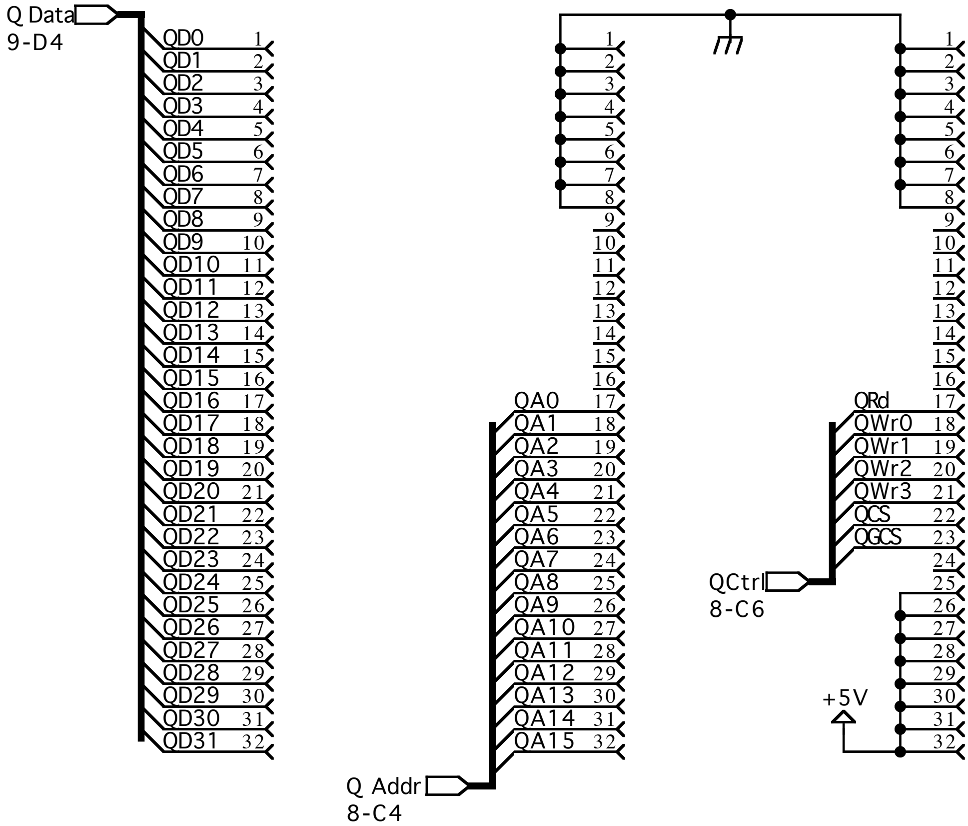
Program Store RAM


RAMSel
11-A3, 8-A4
+5V
74
1D
1CLK
1Q
1Q
RAMSel*
11-A3
1PRE
1CLR
Addr
8-A1, 5-A2, 4-C5
A2
A3
A4
A
B
C
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
138
BRd*
9-A1, 8-A4, 5-D2
G2B
G2A
G1
Port*
7-B5, 5-B3
+5V
1k
+5V
220R
125
AD
9-B1, 6-B5, 4-B5, 1-A3, 1-C5
AD0
AD1
AD2
AD3
IN0
IN1
IN2
IN3
In
11-B4
Q*
5-B2
Q Data En*
9-A3, 8-A5
FS*
5-B2
FS Data En*
9-A6, 8-C5
RAM Control
Input/Output Ports
Threshold
11-C4
374
OC
CLK
Th0
Th1
Th2
Th3
Th4
Th5
Th6
Th7
AD4
AD5
AD6
AD7
Port*
7-A2, 5-B3
Out
11-C1
Out0
Out1
Out2
Out3
Out4
Out5
174
CLR
+5V
Buf Write
8-A5, 5-D2
BWr0
Ctrl Port*
5-B3

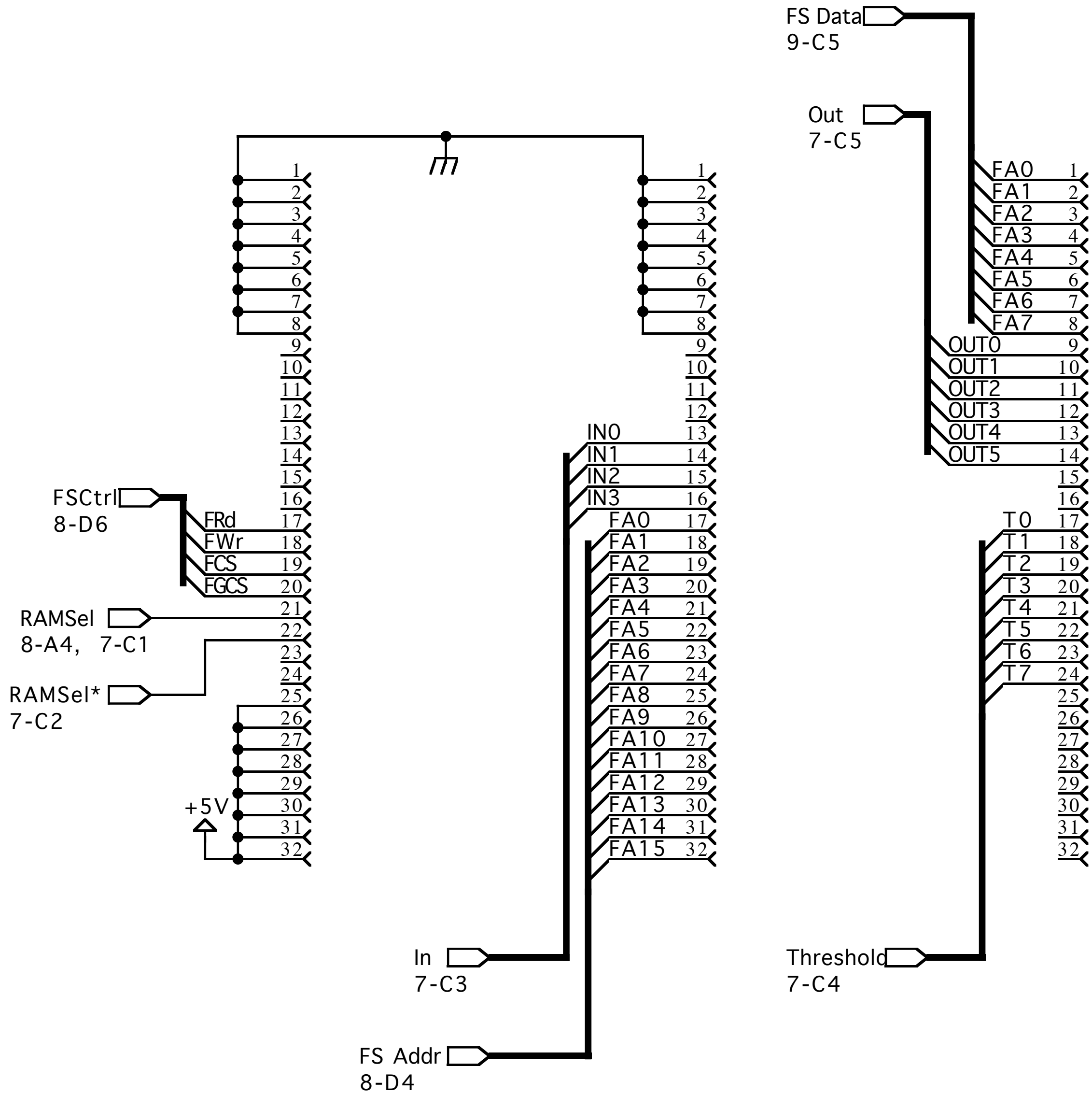

A
B
C
D
1
2
3
4
5
6
Addr
7-A2, 5-A2, 4-C5
+5V
DIR
A2 A3 A4 A5 A6 A7 A8 A9
A0 B0
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
245
EN
QA0 QA1 QA2 QA3 QA4 QA5 QA6 QA7
FA0 FA1 FA2 FA3 FA4 FA5 FA6 FA7
A10 A11 A12 A13 A14 A15 A16 A17
QA8 QA9 QA10 QA11 QA12 QA13 QA14 QA15
FA8 FA9 FA10 FA11 FA12 FA13 FA14 FA15
RAMSel
11-A3, 7-C1
Q Addr
10-B3
FS Addr
11-B4
Address Buffers
BRd*
9-A1, 7-A2, 5-D2
Buf Write
7-A5, 5-D2
FS Data En*
9-A6, 7-D3
BWr0 BWr1 BWr2 BWr3
QRd QWr0 QWr1 QWr2 QWr3 QCS QGCS
FRd FWr FCS FGCS
Q Data En*
9-A3, 7-D3
SRAM*
1-D2
Control Buffers
QCtrl
10-C3
FSCtrl
11-A2



Data Buffers


Q Data
9-D4
QD0 QD1 QD2 QD3 QD4 QD5 QD6 QD7 QD8 QD9 QD10 QD11 QD12 QD13 QD14 QD15 QD16 QD17 QD18 QD19 QD20 QD21 QD22 QD23 QD24 QD25 QD26 QD27 QD28 QD29 QD30 QD31
QA0 QA1 QA2 QA3 QA4 QA5 QA6 QA7 QA8 QA9 QA10 QA11 QA12 QA13 QA14 QA15
Q Addr
8-C4
QRd QWr0 QWr1 QWr2 QWr3 QCS QGCS
QCtrl
8-C6
+5V
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

Q Connector



Framestore (P) Connector